Fully Functional Fine-grain Vertically Integrated 3D Focal Plane Neuromorphic Processor

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***Abstract*—This paper presents the first fully functional fine-grain 3D vertically integrated focal plane system processor, implemented in the 3D interconnection technology of Tezzaron Semiconductors. The processor consists of an array of cells, auxiliar structures and general purpose blocks. The chip can acquire video and apply a series of image processing tasks to each frame employing local computation among cells. The chip has been successfully tested at 50Mhz.**

***Index Terms*—3D integration, focal plane processor**

I. Introduction

Event though the benefits of vertical 3D integration have been shown in the literature [1], few functional experimental prototypes have been reported. [2] and [3] report imagers built with two tiers, where the photodiodes are in one tier and the acquisition electronics are on the other tier. [4] reports a fine-grain DSP processing unit, with electronics in both levels, and [1] reports one wafer with 64 processor cores connected to another SRAM memory wafer; both chips were fabricated using a 130nm process and Tezzaron interconnection technology.

This paper presents the first fully functional fine-grain 3D vertically integrated focal plane system processor, based on the simplicial CNN architecture [5], [6]. The 3D IC has two tiers implemented on the Chartered 130nm technology and Tezzaron interconnection technology. The integrated circuit (IC) consists of an array of cells, where every cell is distributed in the two tiers, together with auxiliar and general purpose computation blocks (see Fig. 1) so that the chip can perform low and medium level image processing operations. The chip has been successfully tested at 50MHz.

II. Architecture

The array is composed by 48×32 elements. The auxiliary computation structures are located on one side of the array, and include: a) a core for nonlinear (piecewise linear) computation; b) a BUS manager; c) a control and decoder control unit; d) a program memory; e) a column adder and an integrator; f) a multiplier and a divider; g) a chain code generator; h) a correlator. The column adder and the integrator are used to calculate the sum of the value of all the pixels in the image. The multiplier and divider, together with the sum of all pixels can be used to calculate several image descriptors. The general purpose structures are an 8051 micro controller and a UART unit.

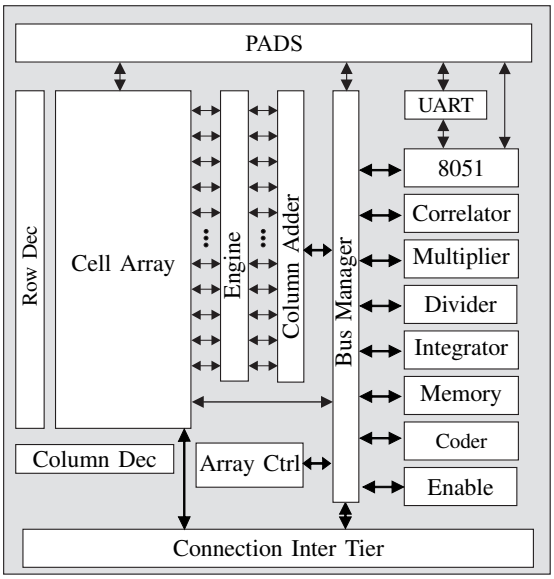

Fig. 1: Block Diagram.

Every cell in the array is composed of the blocks illustrated in Fig. 2, namely, two 7-bit registers, one 7-bit counter, two latches and one multiplexer. There are 9 3D bias per cell. The array computes one column at a time. The pixel value is acquired and converted into a 7-bit digital word in the top tier. Then, it is stored in U register in the bottom tier. During computation, X and U digital words are placed on the bus and compared with a digital ramp running on the internal bus. This is done using the column comparators, and the obtained results are one-bit time-coded (PWM) signals. These value are latched into the F and G latches in the cell bottom tier. Then these two latch values are placed on the bus, and grouped together with the corresponding signals of the 4 local neighbour cells. These 5 values access the 32×1 parameter memory, located on the column array, which are digitally operated by the programmable FoG block, and subsequently added by the counter located in the top tier of the cell. This process is repeated until all columns have been computed.

The IC can work with different pixel resolutions: 7-bit grayscale or 1-bit black/white. The processing time depends on the resolution: black and white images can be processed in 1 or

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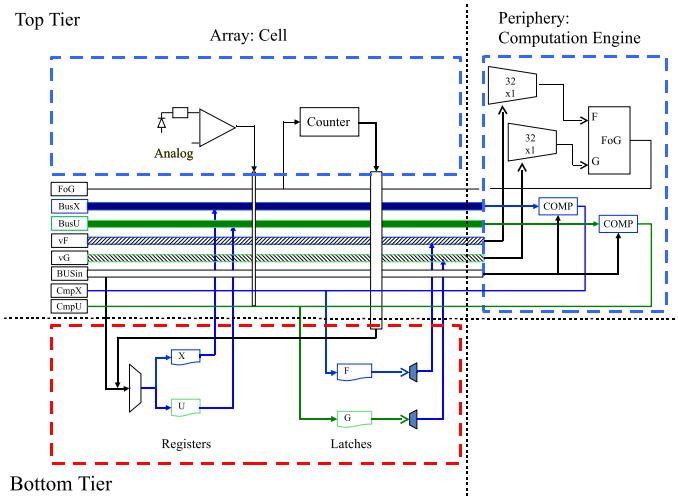

Fig. 2: Cell structure.

2 clock cycles, using one or two registers. Similarly, images of 7-bit pixel resolutions are processed in 64 or 128 cycles. With a clock running at 50Mhz, this architecture can process 375 thousand grayscale images or 25 million black/white images per second.

III. VLSI Implementation and Results

The full chip size is 2mmx2.5mm, the working voltage for the core is 1.5V, and the I/O works at 3.3V. The chip has 70 pads, encapsulated in a PGA85 package.

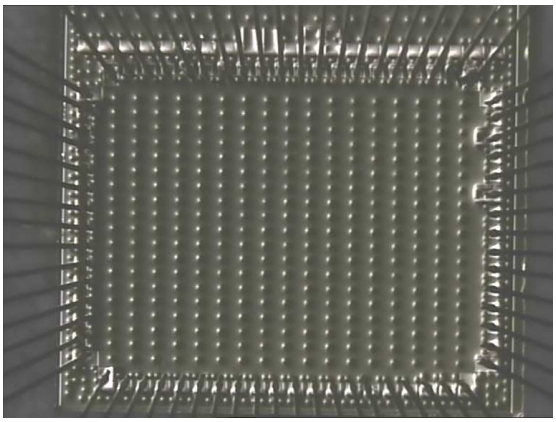

Fig. 3: IC microphotograph.

A test board to control and test the prototype was fabricated. This board is controlled by an FPGA with a microprocessor that communicates with the PC. This test board was designed to send and receive a large number of signals: it can manage 256 8-bit digital input/output ports. The PC send commands to the microcontroller in the FPGA through the UART. The clock frequency in this test was 50Mhz, mainly limited by the test board. Fig. 4 shows a snapshot of an image acquired by the chip and the result of several processing operations applied on the fly by the chip. The left column, from top to bottom, shows: the original image captured by photodiodes; the fixed pattern noise removal with Correlated Double Sampling; a Median filter

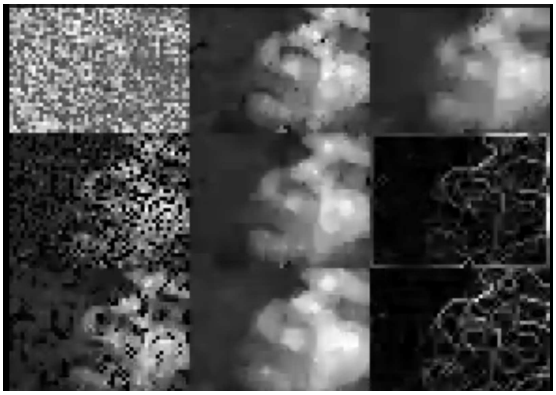

Fig. 4: Image of a face acquired by the chip (Top Left) and outputs from different processing algorithms executed by the chip.

applied to the Center Left Image. The center column, from top to bottom, shows: the image closure, a median filter applied to the closed image; the dilation of the filtered image. The right column, from top to bottom, shows: opening and closing; edge recognition using the difference between the eroded image and the original; edge recognition using the difference between the dilated image and the original. The video captured and processed by the chip is available at [7].

IV. Conclusions

3D technology can be used at present to build complex systems. We have provided experimental evidence of a full working prototype of a system that acquires images, and performs A/D conversion plus local nonlinear computation at the pixel level, with a fine-grain design methodology. In addition, the system has blocks that can be used to perform mid and high level processing tasks.

Acknowledgment

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