# Silicon on Sapphire CMOS for Optoelectronic Microsystems

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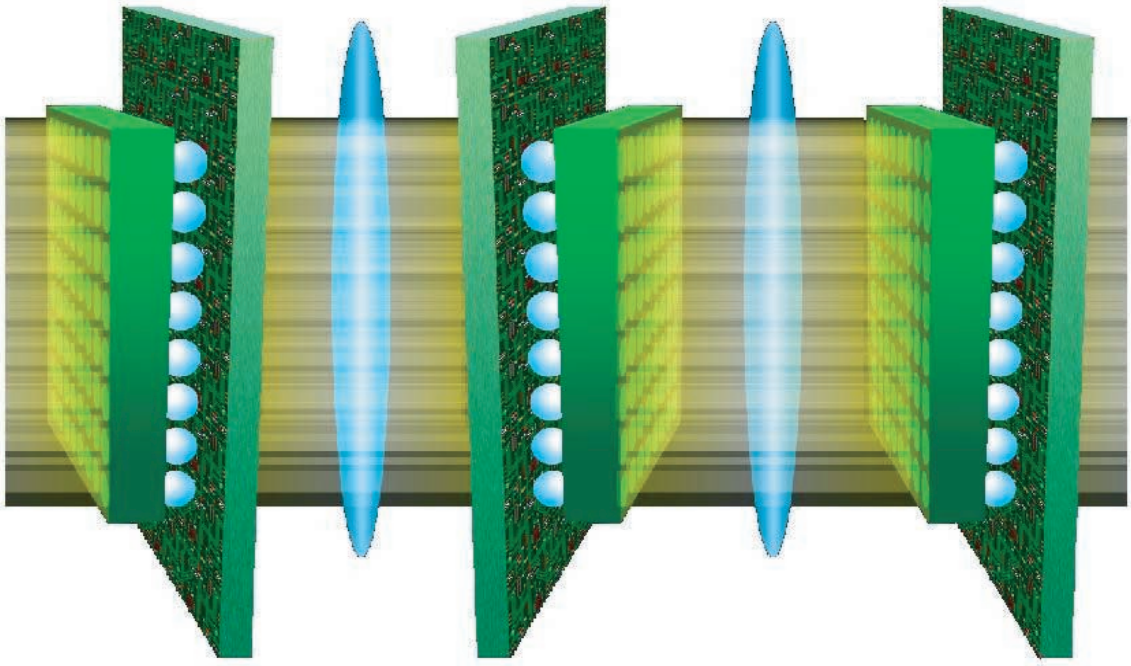

*Figure 2. Parallel interconnect cascade information processing architecture employing through-the-substrate optical vias and high-speed CMOS processing circuits.*

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## Introduction

Packaging has become an increasingly important cost issue in today's highly competitive microelectronic technology markets that demand cost-effective integrated solutions and systems on a chip. Technical challenges related to packaging are often considered independently of the device and integrated circuit fabrication processes, and technological advances in the two fields have traditionally followed separate and independent paths. The importance of packaging is even greater in the emerging optoelectronic VLSI technologies where the integration of photonic elements with high-speed silicon CMOS VLSI opens the way to subsystems for interconnects in local computer networks, intra-computer and even intra-die applications [1].

In this article we report on a hybrid integration approach that represents a paradigm shift from traditional optoelectronic integration and packaging methods. A recent metamorphosis and wider availability of silicon on sapphire CMOS VLSI technology is generating a great deal of excitement in the optoelectronic systems community as it offers simple and elegant solutions to the many system integration and packaging challenges that one faces when employing bulk silicon CMOS technologies. In the bulk silicon CMOS processes that are used for high-speed interface electronics the substrate is absorbing at both 850-nm and 980-nm wavelengths, necessitating complex and expensive integration procedures such as VCSEL substrate removal to enable the implementation of optical vias through the substrate [1].

Working together, the optical transparency of the sapphire substrate, its superb thermal conductivity and the excellent high speed device characteristics of silicon-on-sapphire CMOS circuits make this technology an excellent choice for cost effective optoelectronic *Die-AS-Package* (DASP) systems (Fig. 1) and for implementing optical interconnects for high performance computer architectures (Fig. 2).

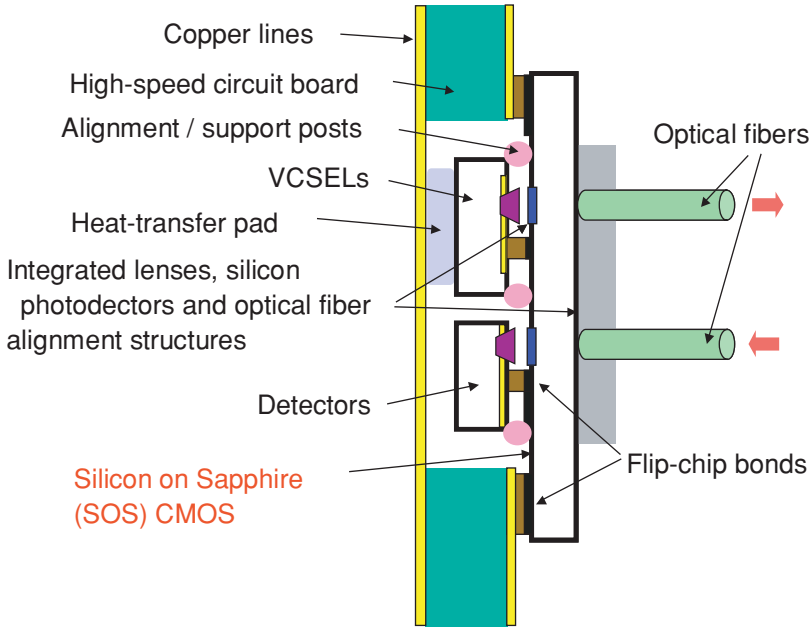



*Figure 1. Die-as-package optoelectronic module comprised of a silicon on sapphire CMOS die, active photonic elements (detector and VCSEL arrays) and passive photonic waveguides and couplers that direct light into bundles of optical fibers.*

What is perhaps even more important, packaging and input/output interface issues can now be addressed at the CMOS wafer fabrication level where input/output structures can be accurately defined, optimized and processed using lithographic techniques, eliminating problematic die post-processing and packaging-related optical alignment issues.

## Ultra-Thin Silicon-on-Sapphire CMOS

Silicon on insulator (SOI) is emerging as a mainstream technology poised to become the standard for deep sub-micron VLSI [2–3]. Devices with $f_{max}$ near 100GHz have been reported in sub-tenth-micron silicon on insula-

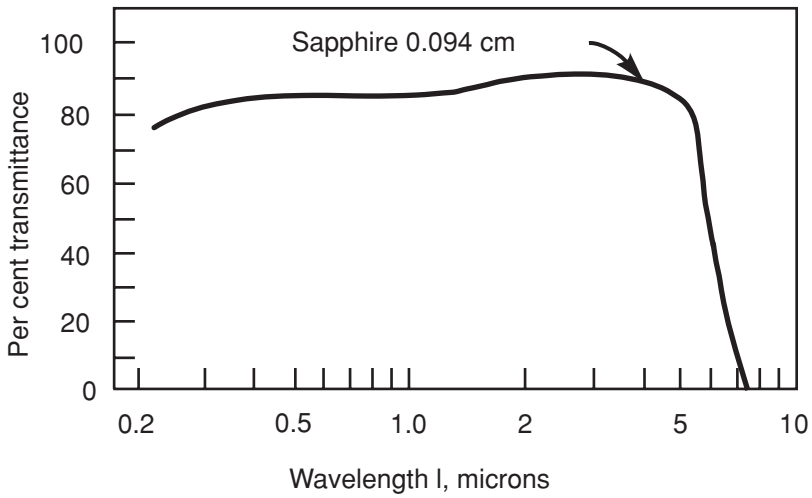



*Figure 3. Optical transmittance of sapphire (adapted from [6]).*

tor CMOS [4]. In comparisons between bulk CMOS and silicon on insulator at similar power levels, there is up to a 300 per cent performance gain using the technologies that employ devices fabricated on insulator [5]. The advantage of SOI processes over bulk CMOS are:

- reduced short channel effects
- reduced parasitic capacitances
- reduced body effect (transconductance degradation)
- reduced latch-up
- reduced leakage currents due to lower area parasitic junctions
- ultra low noise figure

Silicon on sapphire CMOS technology is a close cousin to the more popular silicon/silicon dioxide based SOI technologies that use sapphire-aluminum oxide ($Al_2O_3$) as the substrate. This is an excellent electrical insulator, and its thermal conductivity is higher than silicon dioxide. Moreover, as can be seen from the experimental data in Fig. 3, it is practically transparent in wavelengths ranging from the ultraviolet (200nm) to infrared (5500 nm).

Peregrine's 0.5 micron ultra-thin silicon on sapphire CMOS process represents a breakthrough in silicon on

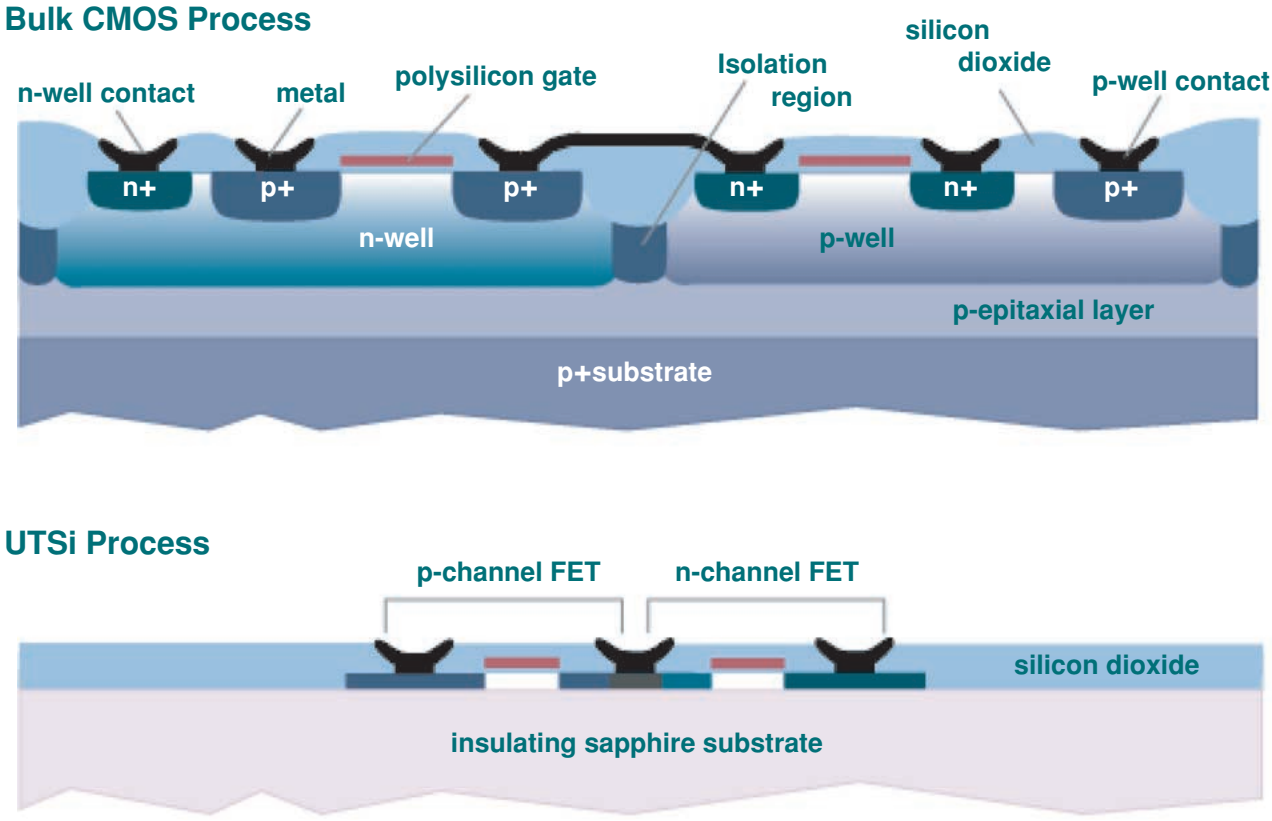



*Figure 4. Ultra thin silicon on sapphire CMOS process compared to a standard bulk CMOS Process.*

sapphire technology in that the thickness of the silicon is only 100 nm as opposed to older technologies that employ silicon a few microns thick (see Fig. 4). Peregrine's technology has been added to the list of processes that are available from MOSIS [7] over two years ago, and hence it is readily available to the commercial and research communities for experimentation and rapid prototyping.

Peregrine's process available from MOSIS is a regular 0.5 micron single poly three metal CMOS process, but offers the circuit designer six types of MOSFETs, as compared to the two types available in almost all other commercially available CMOS processes (see Fig. 5). For each device type (NMOS or PMOS), a designer has a choice of threshold voltage: regular (0.6 Volts), low (0.35 Volts), and zero (0 Volts). Devices are normally fully depleted three terminal structures but the doping of the regular n-type and p-type devices is such that they can be operated as partially depleted and hence as four terminal MOS structures. The fully depleted devices with their intrinsic lower threshold, higher normalized transconductance and reduced parasitics can be used in high performance analog blocks such as transimpedance amplifiers and voltage amplifier systems and in RF high frequency circuits.The partially depleted devices with body contacts can be used in low frequency circuits and bias blocks as well as other circuit topologies that necessitate a four terminal MOS structure.

The availability of devices with three different threshold voltages makes the fabrication process a little bit more complex, but it offers the circuit designer new challenges and opportunities, especially in high speed mixed analog/digital circuits.

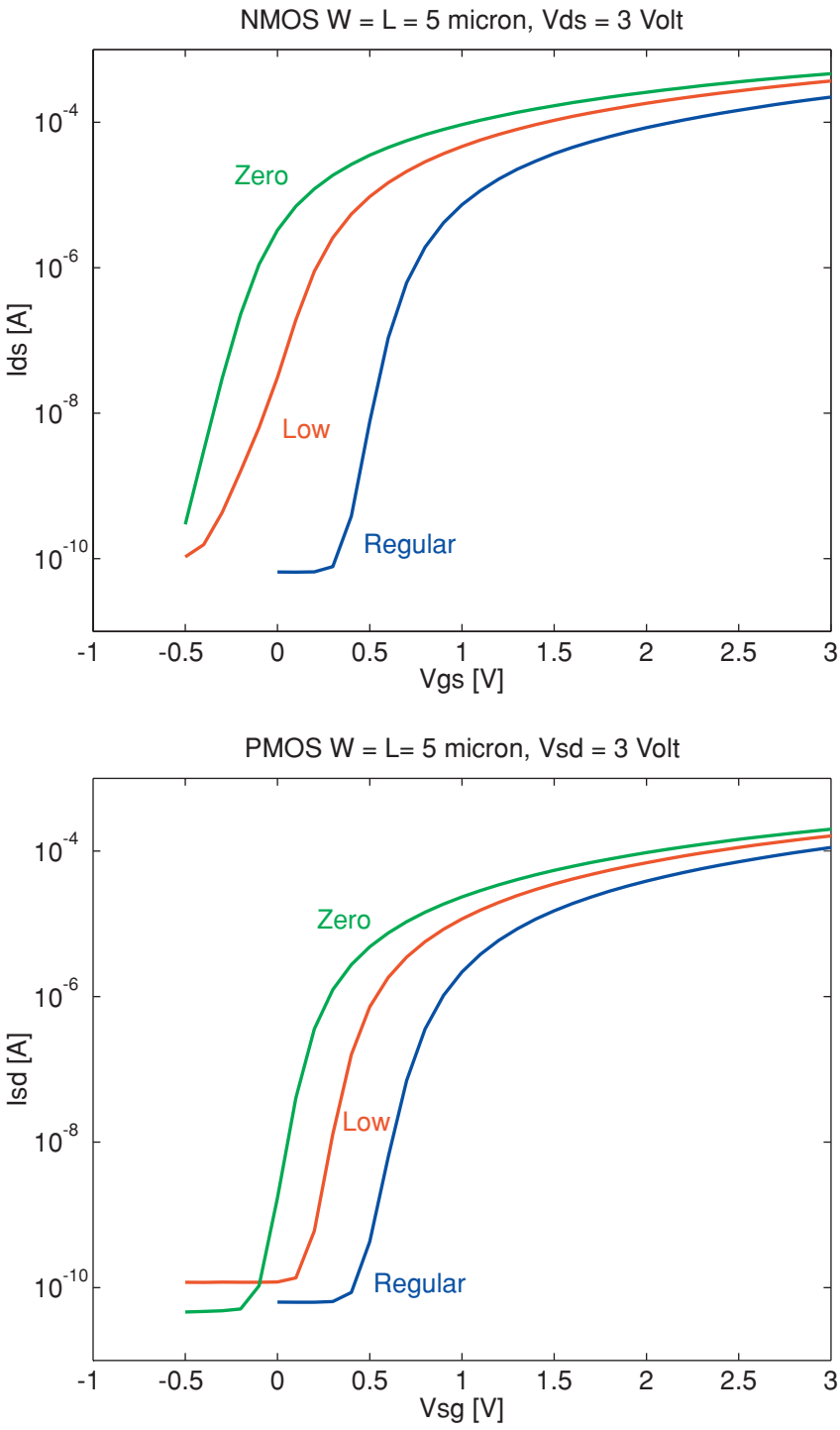



*Figure 5. Typical transfer characteristics for the six types of three terminal devices available in the Peregrine SOS process.*

## "Kinky" Transistors

In silicon on insulator processes, MOS transistors are formed as islands of silicon on the insulating substrate, and hence they are fabricated without a body connection. This results in undesirable floating body effects, such as

Note: field oxide not shown.

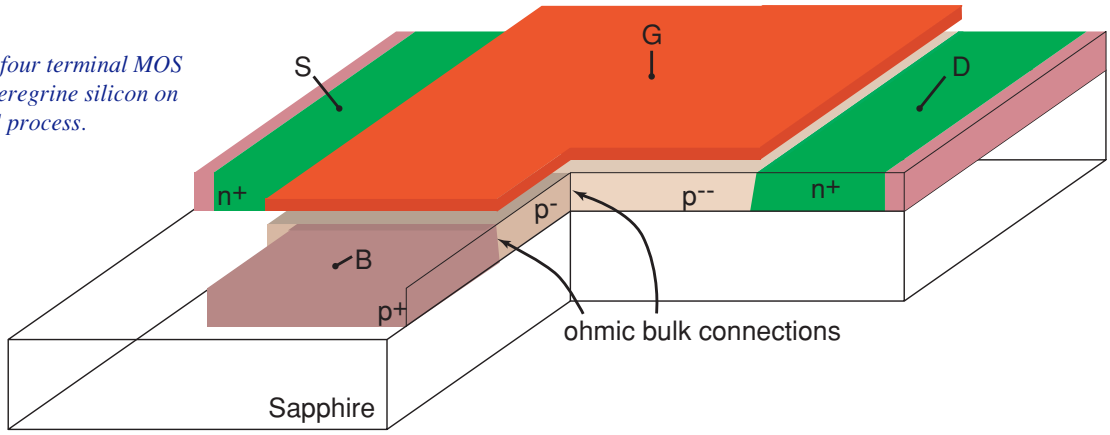
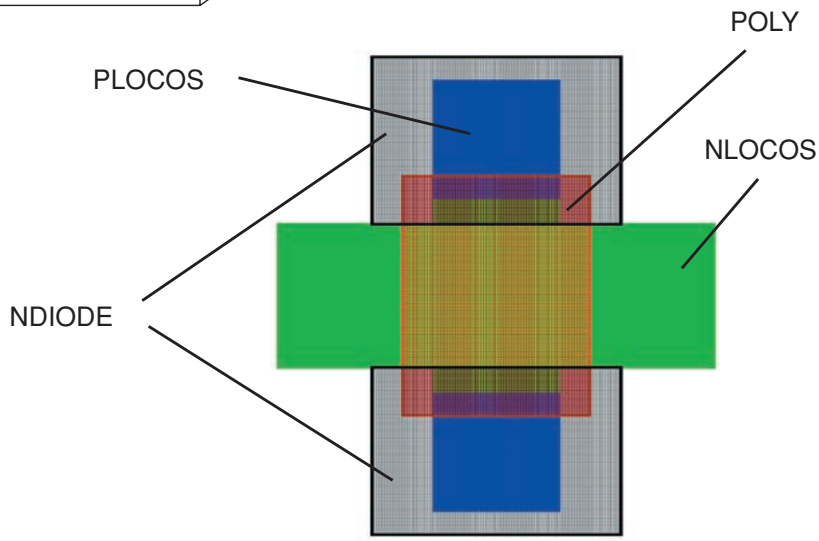



*Figure 6. Structure of the four terminal MOS device designed for the Peregrine silicon on sapphire CMOS process.*



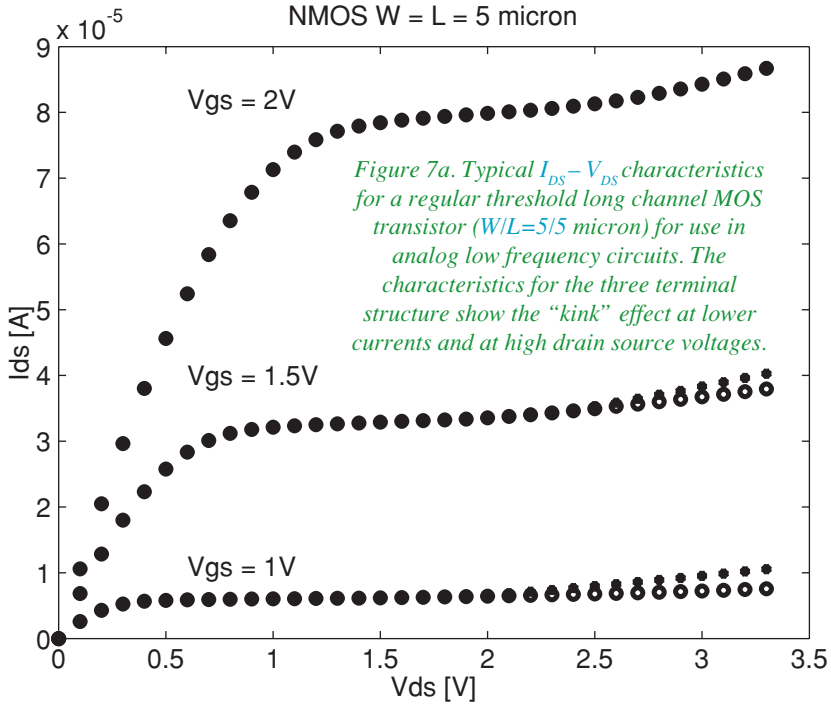




*Figure 7a. Typical $I_{DS} - V_{DS}$ characteristics for a regular threshold long channel MOS transistor (W/L=5/5 micron) for use in analog low frequency circuits. The characteristics for the three terminal structure show the "kink" effect at lower currents and at high drain source voltages.*

the *kink* effect [5]. At low frequencies, majority carriers generated by impact ionization collect under the channel of the transistor, raising the body potential and lowering the transistor's threshold voltage. This feedback effect accounts for a *kink* in the output characteristics of the devices. In a technology where the devices are fully depleted, the kink effect is minimal. In the Peregrine process this is true for the low and zero threshold devices that have lighter doping in the channel and thus are fully depleted. This is not true for the regular threshold devices. A four terminal structure such as the one depicted in Fig. 6 above provides a solution to the missing body problem as evident from the data in Fig. 7.

## Integrated Optoelectronic Module

We exploit the transparent property of the substrate in an optoelectronic module by flip-chip bonding industry standard, commercially available surface emitting lasers [8] on the surface of the silicon die and directing the light from the VCSELs through the substrate. This integration process offers a simple and straightforward method for implementing optical vias through the substrate, that in turn enable similar modules to be readily stacked and communicate with each other bi-directionally without the need of complex optics (see Fig. 2).

The mature 850-nm GaAs/AlGaAs-quantum-well vertical-cavity surface emitting lasers (VCSELs) are commercially available [8] in one dimensional arrays with aggregate bandwidths in excess of 15 Gb/s, aimed at the data communication and switching fabric infrastructure. 2D arrays of 850-nm VCSELs have also been developed in the research community [9]. The 850-nm VCSELs are front emitting structures because the substrate is not transparent at the emitting wavelength. The 980-nm InGaAs/AlGaAs back emitting VCSEL technology is maturing rapidly and is available in two dimensional arrays [9] that can be readily flip-chip bonded to CMOS circuits [10] and employed in advanced architectures for image processing, because the VCSEL substrate is transparent at the emitting wavelength of 980-nm. The integration process is depicted in Fig. 8.

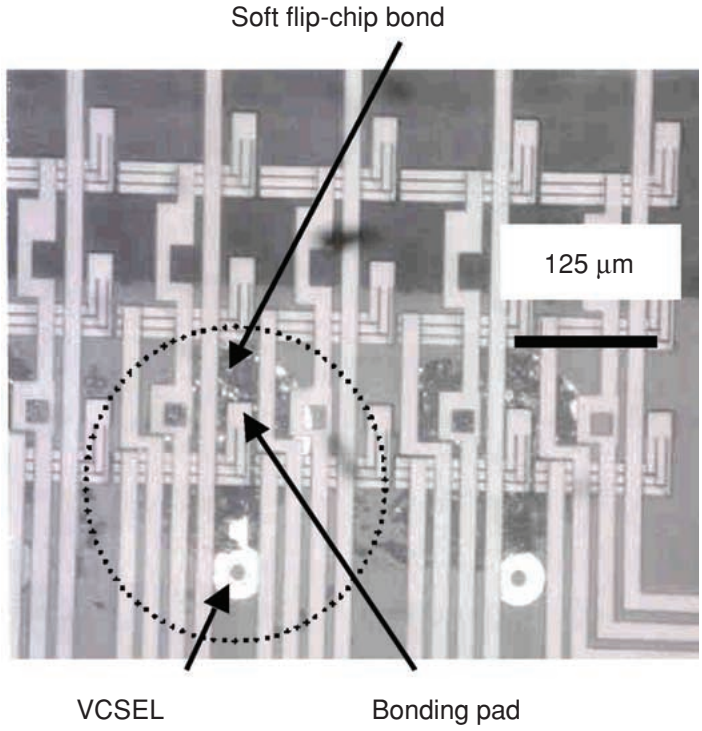



*Figure 8. Photograph of the integrated module taken from the backside of the SOS CMOS die.*

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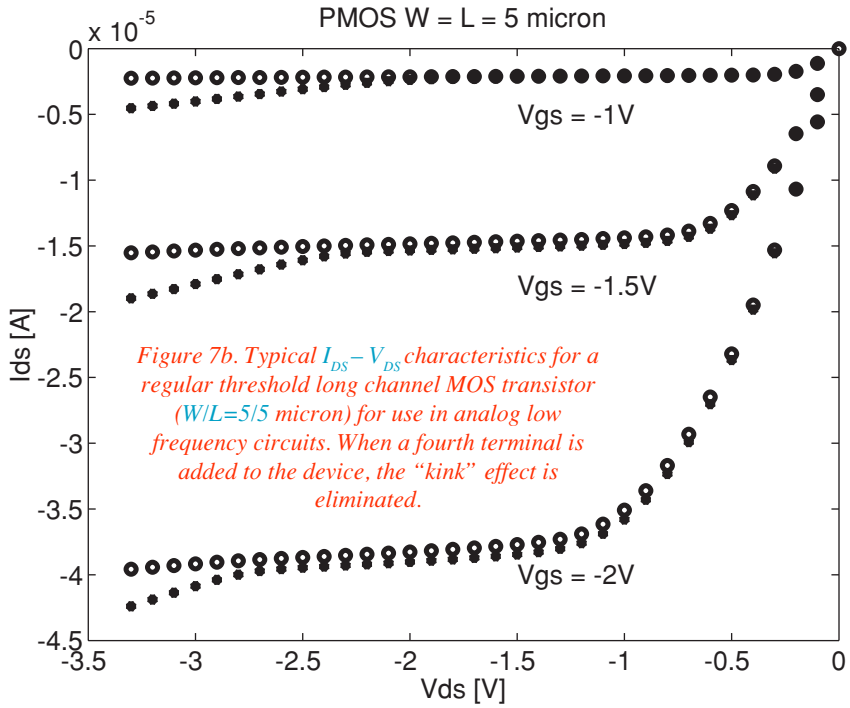


*Figure 7b. Typical $I_{DS} - V_{DS}$ characteristics for a regular threshold long channel MOS transistor (W/L=5/5 micron) for use in analog low frequency circuits. When a fourth terminal is added to the device, the "kink" effect is eliminated.*

Circuits were fabricated in the 0.5 micron, 3-metal, 2-poly, silicon on sapphire CMOS process through the MOSIS foundry [7]. The die, as received from MOSIS, was optically polished on the front surface but not on the backside, resulting in severe light loss due to scattering from the back surface. This problem was solved by using index matching wax to mount the die on a glass cover slide. The glass cover slide was then mounted on a blank lithography mask and placed upside down in the mask aligner. Conductive epoxy was applied to each of the bonding pads of the VCSEL die that was subsequently placed on the wafer of the mask aligner. Drops of UV curable epoxy were also placed at the corners of the die. After optical alignment the blank mask with the SOS CMOS die was lowered to make contact with the VCSEL die, and the two dies were mechanically bonded together by exposing the assembly to UV light. After exposure the assembly was placed in a convection oven and the conductive epoxy was cured for an hour at a temperature of 60º C.

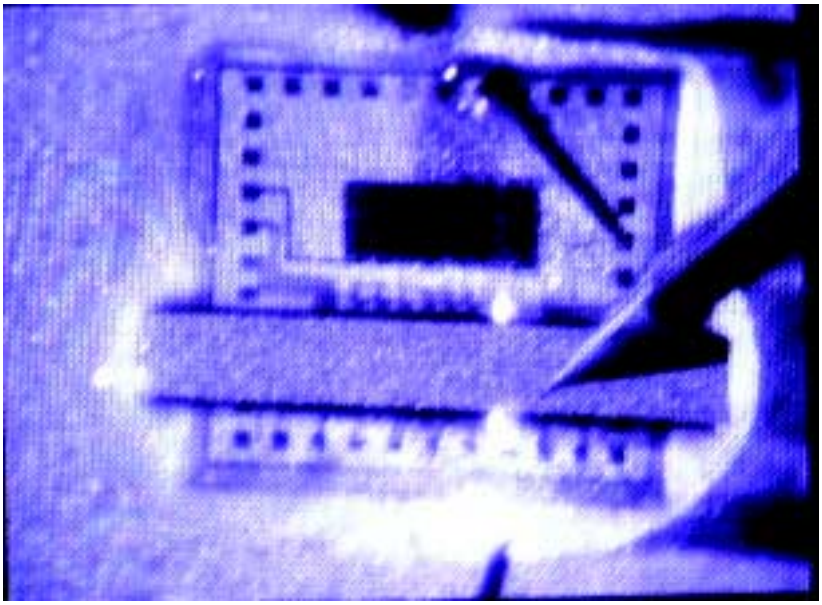

*Figure 9. The assembled module probed so as to activate one of the VCSEL's in the array. The light is emitted downwards and is specularly reflected from the stage of the probing station.*

## Testing

The hybridized module was tested for functionality by probing the die and selecting individual VCSELs bonded on CMOS drivers in an X-Y addressing matrix. Fig. 9 shows one VCSEL device in ON while the others are OFF. The flip-chip bonding method that we employed yielded low resistance bonds between the aluminum pad on the SOS CMOS die and the gold pad on the VCSEL die.

## Ultra-Thin Silicon for Lean and Mean Circuits!

The quality of the "soft" flip-chip bonding was further evaluated by testing the flip-chip bonded devices on fan-out test pads at high frequencies. An HP 9815 network analyzer together with a VCSEL bias circuit was used to drive the VCSELs on the hybridized assembly. The light emitted from the backside of the silicon die was focused on a high speed photodector (Thor Labs DET210) whose output was monitored using a digital oscilloscope (Tektronix TDS380). Data rates in excess of 1Gb/s were obtained, demonstrating the high speed integrity of the process. In another series of high frequency testing, ultra-thin silicon CMOS buffers were wire-bonded to VCSELs and operated at frequencies as high as 6 GHz, (exceeding the cut-off frequencies of the VCSELs). We have fabricated both transmitter and receiver array test circuits in the 0.5 micron, 3-metal, 1-poly, ultra-thin silicon on sapphire CMOS process through the MOSIS foundry [7].

The test results for a typical receiver are shown in Fig. 10. The receiver, a 5 stage differential architecture [11] is tested with an MSM

bonded on the input and with a light source driving the MSM detector. The receiver shows open eye diagrams at 1Gb/s with 5 mW power dissipation and 3.3 volts supply.

## Acknowledgements

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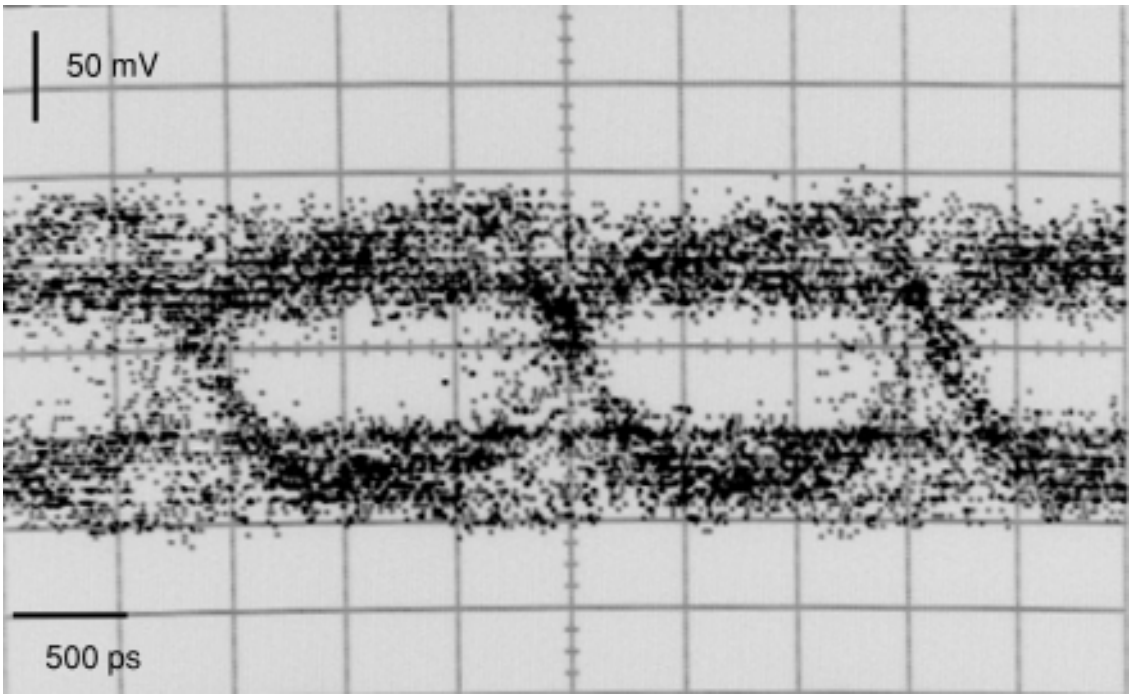


*Figure 10. Eye diagram for an ultra-thin silicon on sapphire CMOS optoelectronic receiver circuit.*